TECHNICAL NOTE

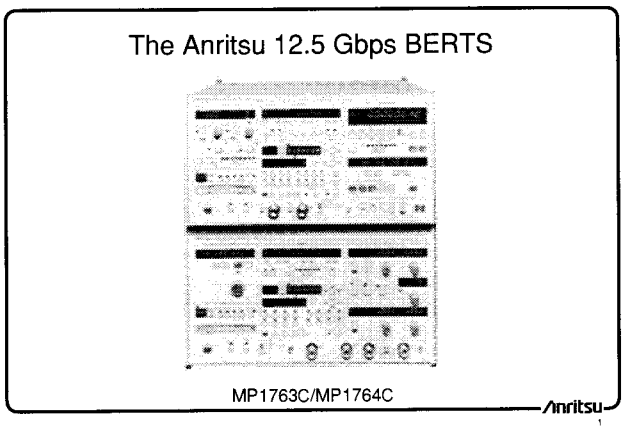
MP1763C/MP1764C

12.5 Gbps BERTS

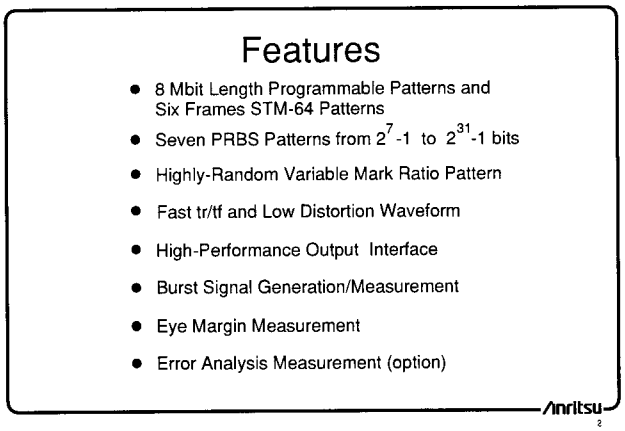
MEASUREMENT SOLUTIONS

ANRITSU CORPORATION

The MP1763C/MP1764C 12.5 Gbps Bit Error Rate Test Set (BERTS) was developed by Anritsu to support ultra-high speed pulse technology. The BERTS is constructed of a Pulse Pattern Generator (PPG) and an Error Detector (ED). The 12.5 Gbps BERTS shares functions and GPIB commands with the 3 Gbps BERTS, allowing compatibility of application software. This BERTS delivers enhanced performance in a design which anticipates future user requirements.

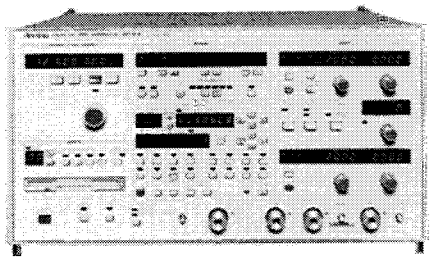


The 12.5 Gbps BERTS has the following features.
* A 8 Mbit programmable pattern capable of generating six STM-64 frames.
* A programmable frame sync capability in the error detector to enable fast synchronization on the programmable word.
* PRBS patterns from 2^7-1 to 2^{31}-1 bits long can be generated; in addition, the patterns can be generated with variable mark ratios.
Also, a burst signal can be generated and measured.
* Output waveforms (clock and data) with low distortion, fast rise and fall times, variable offsets and amplitudes, and differential drive.
Three error detection modes; omission, insertion and total.



This is the external view of the MP1763C front panel. The MP1652A panel is nearly same looking as this. At a glance, it looks like there are many operating keys and knobs and that the operating procedure is complex.
Although the instrument is extremely flexible the front key panel is divided into functional blocks with only a few keys per block to allow "intuitive" operation.
Besides, there are only a functions in each operation, because of the concept that it has been given to splitting up multiple functions.
These are used to set the input conditions for the device under test. Operation is extremely convenient for setting the most suitable parameters such as input level, offset and delay.

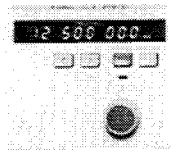
External View of MP1763C PPG



Anritsu

Each member of the Anritsu MP1763C has an internal clock generator as an option.
Two switches are provided so that the lowest displayed digit can be blanked when there are too many digits at 1 kHz resolution.
The switching response time and SSB phase noise characteristics do not vary according to the resolution setting.
The SSB phase noise is very important specification. Anritsu's -70 dBc/Hz at 12.5 GHz is sufficient for almost all applications.

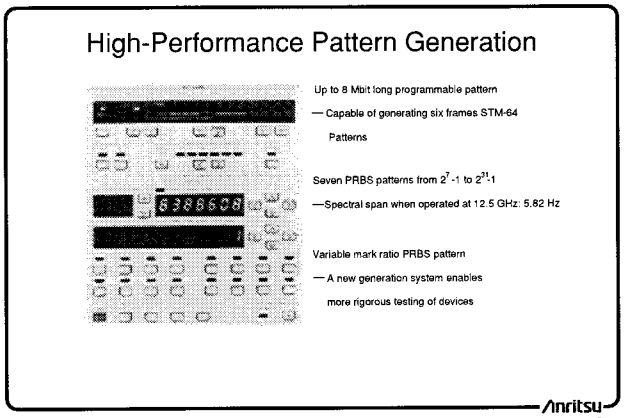
Built-In Synthesized Clock Generator



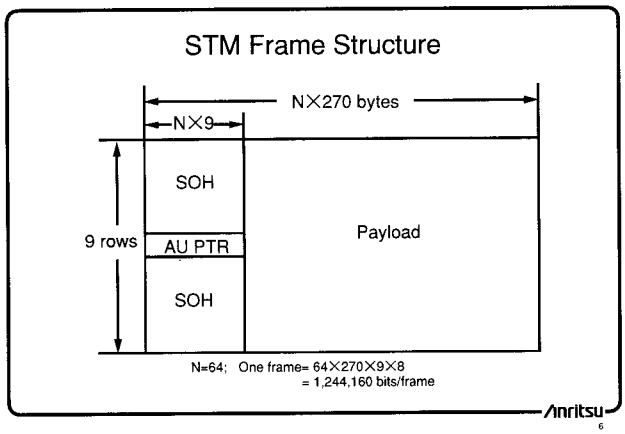
- 1 kHz/1 MHz Step Setting
- -70 dBc/Hz 10 kHz offset SSB Phase Noise

Anritsu

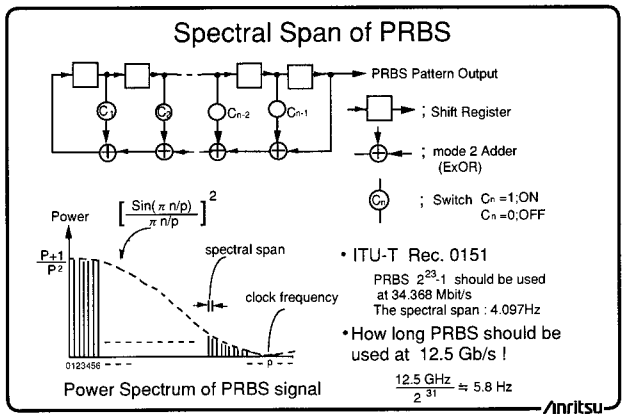
This is the functional block for the pattern generator section.
Two of the main features are that a 2^{31}-1 PRBS pattern can be generated as well as a programmable pattern with a length of up to 8 Mbit.
In addition, the variable mark ratio pattern has high randomness. This signal provides a more accurate characterization of the DUT.



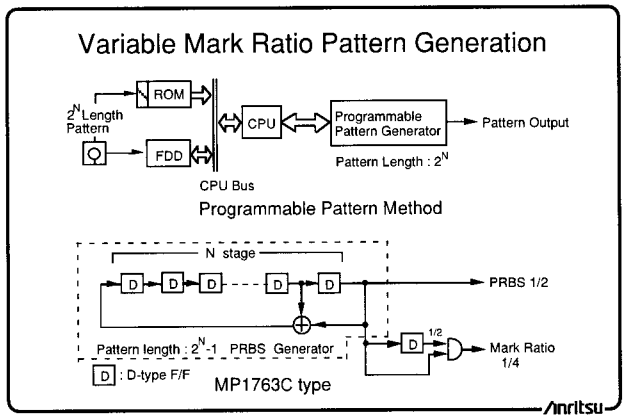
This shows the reason why is a 8 Mbit long pattern is required. This diagram shows an STM-N (STS-3N) signal frame construction. Basically, it is 9 rows and 270 columns; when N=4, 64, etc. The number of lines is 270 multiplied by N.
Consequently when examining an STM-64 signal N=64 and the length of 1 frame becomes: 9 rows×270 columns×64×8=1,244,160 bits. It is best for the hardware composition of the pattern generator section if the generated bit length is to the square power so the PPG has been made to generate a 8 Mbit pattern so the six frames 1.24 Mbit can be easily accommodated.



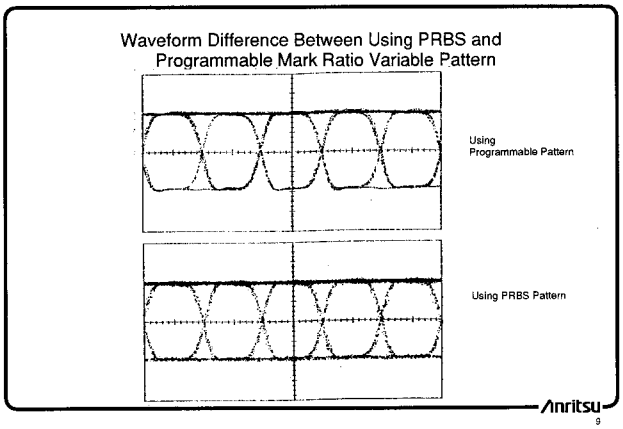
Why is 2^{31}-1 PRBS pattern required ?. The PRBS circuit is composed of a shift register and an exclusive OR. The PRBS signal cycle P is fixed according to the number of steps in the shift register. And when the number of steps is N, it becomes 2^N-1, ITU-T Rec O. 151 recommends using a signal with a cycle of 2^{23}-1 bit length (N=23) for testing 34.368 Mb/s the 3rd order of European hierarchy transmission circuits.
The PRBS signal spectrum is divided into frequency intervals of P. This figure shows the spectral span and the spectra power on the $(\sin(\pi n/p)/\pi n/p)^2$ envelope.
The spectral span is very important for a circuit evaluation. If the span is wide, it becomes an easy signal for DUT to process. If the clock frequency is increased and the PRBS cycle remain the same, the spectral span increases. In order to simulate as close to a random sequence of data the spectral span must be kept as narrow as possible.
In ITU-T Rec O. 151, the spectral span is 4.097 Hz; to maintain this value at 12.5 Gb/s, the PRBS must be a length of 2^{31}-1.



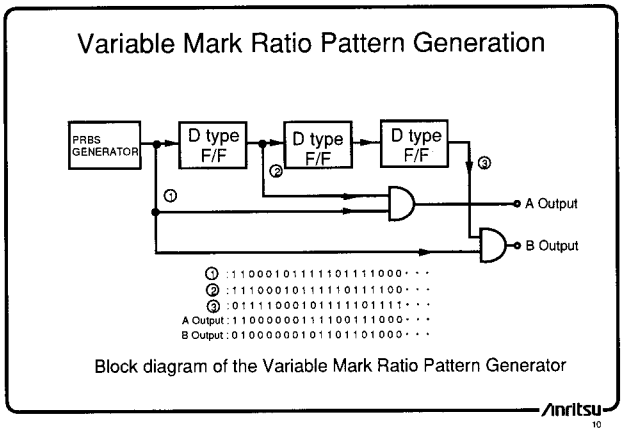
The variable mark ratio pattern generation is an extremely important function of a PPG. This BERTS family has the capability of creating a PRBS pattern with variable mark ratio. there are two generation method of variable mark ratio pattern one providing with programmable patterns and the other using PRBS pattern.
The advantages and disadvantages of these two methods are compared below.
The method for generating the variable mark ratio pattern using the programmable pattern function cannot generate a variable mark ratio pattern having a pattern length longer than the programmable pattern length.
The patterns have been generated by previous computation in a computer and the result is stored in the ROM firmware or on floppy disk and is loaded to the programmable pattern generation section.
By contrast, the method for creating the variable mark ratio pattern with the PRBS gives a delay to the PRBS output pattern at first. Then, a 1/4 mark ratio pattern is created by ANDing the original PRBS pattern with this delayed pattern.
By using this method, a mark ratio pattern can be generated up to a sequence of 2^{31}-1. The PRBS method is superior for generating longer patterns.



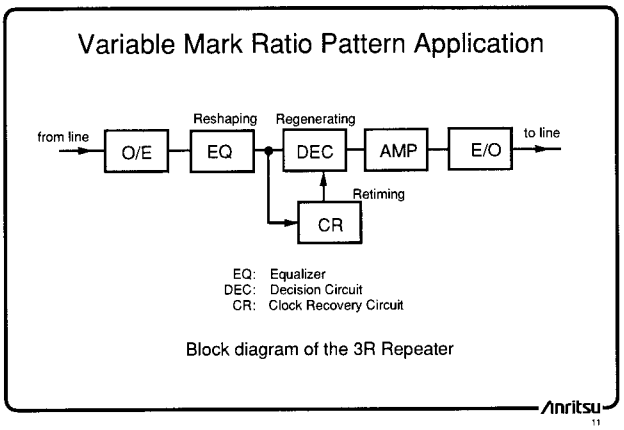
Also, the measurement pattern must have a secure randomness for the pattern cycle. By using the programmable pattern method, the cycle becomes 2^N as already described before, but the 2^N value has a lot of factors. What is the meaning of this ?. This can be clarified from the waveforms. The upper one has a pattern equivalent to the 2^{10} cycle variable mark ratio pattern which was loaded from firmware.
The lower one is the pattern created with a 2^9-1 PRBS pattern. The cycle at 1/32 clock sync pulse on an oscilloscope was hard copied. At a 2^{10} pattern. there are base line gaps here and there. However, this is not observed at 2^9-1. The meaning of this is that 2^{10} and 32 have common factors. 2^9-1 and 32 do not have common factors.



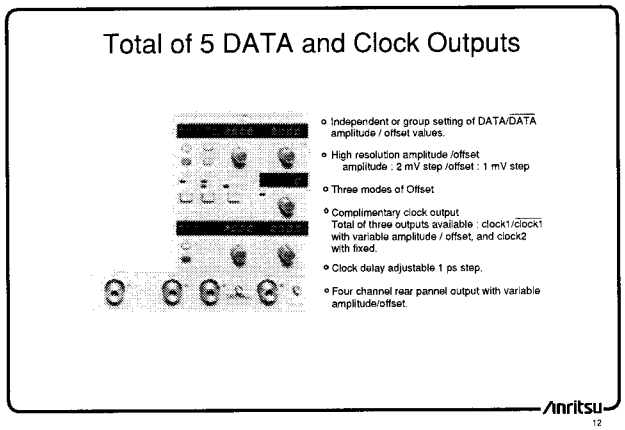
In Anritsu's MP1763C, there are even two methods built-in for generating variable mark ratio patterns using PRBS.
In the first, a 1-bit delay is provided by using the logical AND method. In the other method, a 3-bit delay is provided by logical AND.
With the 1-bit delay, a 101 pattern does not appear: it is always a 1001 pattern with two or more sequential 0s. On the other hand, with the 3-bit delay method, the 101 pattern appears. So we can say that the 3-bit delay pattern method has higher randomness than the 1-bit delay pattern. The 1-bit method is compatible with the Anritsu 2 Gb/s MG642A PPG pattern.
The 3-bit method has been adopted for the new pattern this time.



Both the 1-bit and 3-bit delay methods have application advantages. This diagram shows a block diagram of a 3R optical repeater. The three Rs mean the three functions: Reshaping, Regenerating and Retiming.
With the 3-bit delay pattern, the pattern contains 101. Since this pattern has high-frequency components, the pattern becomes a signal for severe evaluation of the reshaping and regenerating functions.
On the other hand, since the pattern created using the 1-bit delay pattern has lower randomness than the 3-bit method: longer strings of ones and zeros are generated. Also, in one cycle of the generated pattern, there are many maximum 0 continuous sequences. This is a severe test signal for the Retiming function including the Clock Recovery Circuit.



This is the PPG output section. There are five data and clock outputs with various functions.
Independent values can be set for the offset and output amplitude for both DATA and $\overline{\text{DATA}}$.
Also, the resolution is 1 mV and 2 mV, respectively. If independence is not required, tracking can be implemented. The clock outputs are complimentary CLOCK1 and $\overline{\text{CLOCK1}}$.
Furthermore, another CLOCK2 output with a fixed offset and amplitude is available.
Clock delay is provided with resolution of 1 ps.



In Anritsu's MP1763C, both data output and clock output have complete 50-ohm back termination (source matching). For this reason. waveform deterioration due to impedance mismatching is minimized.

There are various types of back termination (source matching) circuits, but some types of circuit influence the output waveform in case of impedance mismatching.

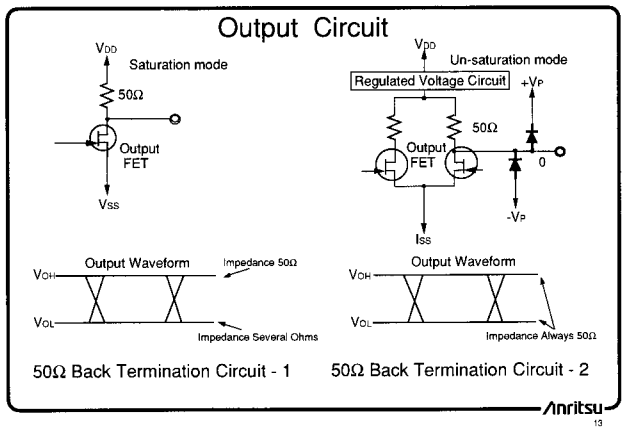
Concerning with the circuit shown on the left.

(In HIGH state (output FET off), output impedance is 50 ohms)

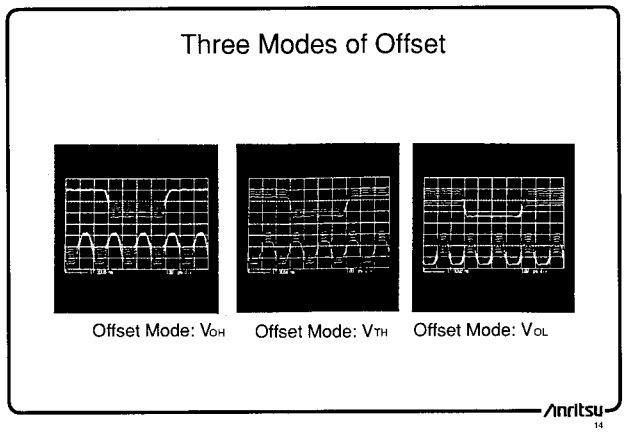
(In LOW state (output FET on), output impedance is low)

This cannot be said to have complete 50 ohm back termination (source matching).

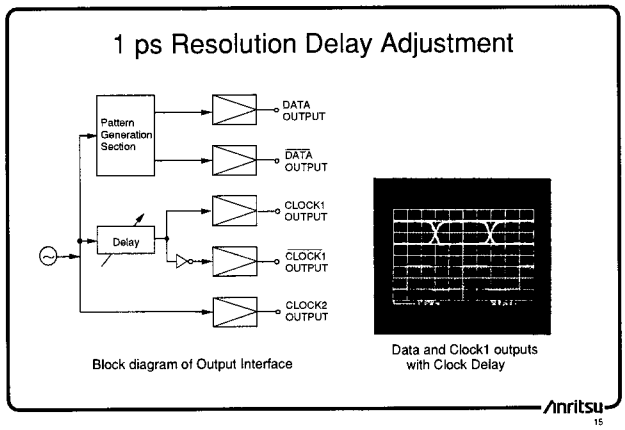
In contrast, Anritsu's PPG output circuit as shown on the right, ensures that the output impedance is 50 ohms in both states. In addition there is a protection circuit that protects the output circuit from exceptional external input voltages.



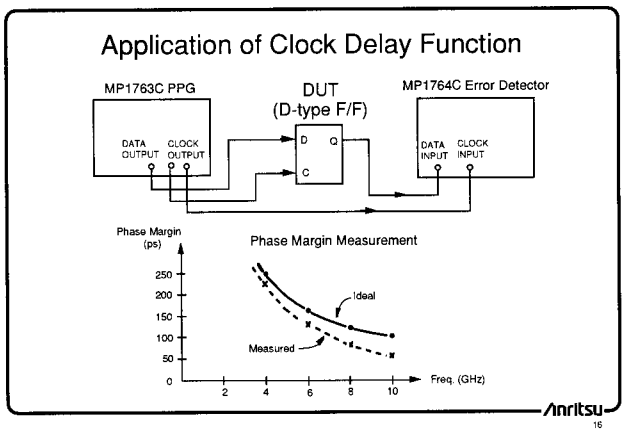
There are three offset modes. The offset voltage reference point can be selected from V_{OH}, V_{TH} and V_{OL}. This function is not only useful for R & D; it is also very useful for testing semiconductors.



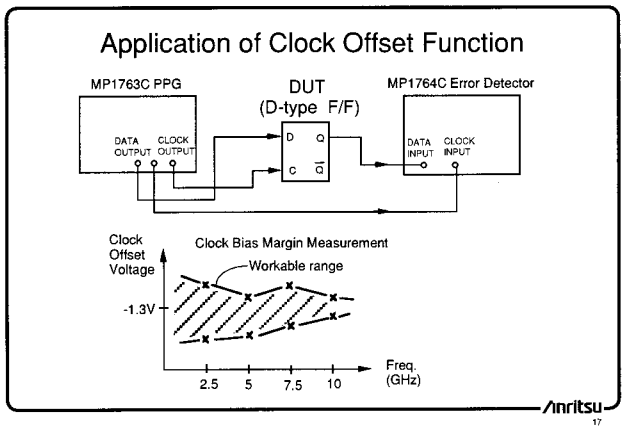
The left figure is the output interface block diagram; the right photograph shows the view when the delay is changed. The delay setting resolution is 1 ps.
Users have asked for continuous variability rather than step variability. Because the delay is controlled by the CPU it cannot be truly linear but the 1 ps resolution will meet the requirements of the most demanding of customers.
There are two delay methods, one mechanical and the other electrical.
However, with electrical delay, there is a possibility of interruption as electrical switches are used when the delay is changed. If interruption occurs the synchronization is lost. With Anritsu's mechanical delay method, interruptions are not generated and sync loss does not occur with changes in delay.



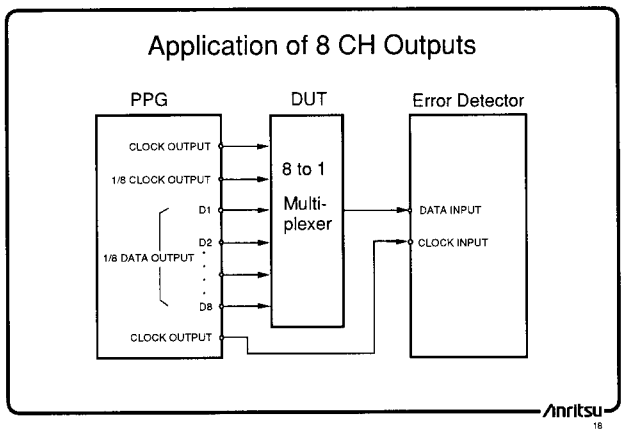
This shows the clock delay function application.
The clock delay is varied and the phase margin of a D type F/F is measured. D type F/F, inherently has a setup and hold time for the data applied.
If a D type F/F were ideal, the setup and hold time would be zero and the phase margin would be the reciprocal of the clock frequency. In reality the F/F setup and hold time is limited. The actual phase margin is obtained by subtracting these times from the pulse cycle. At 12.5 Gb/s, the data pulse width is 80 ps. For phase margin measurement, 10 ps or 5 ps resolution is insufficient; 1 ps resolution is required.
This function of a BERTS is critical in a production environment when automation is necessary.



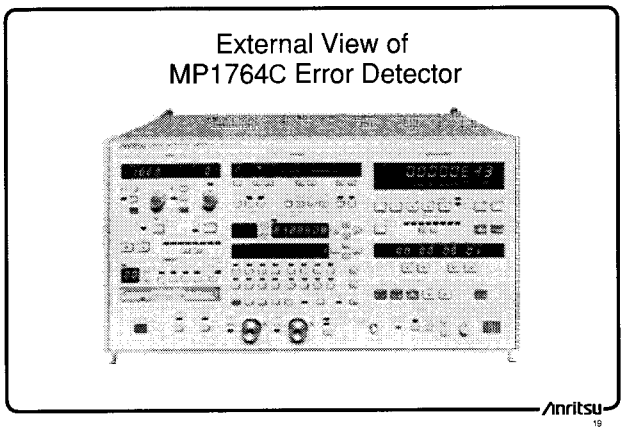
The clock bias margin is equally important as the phase margin. These evaluation items are the most important item for evaluating the maximum operating rate of the DUT. If the DUT is an IC with an ECL interface, choose the V_{TH} reference point for the PPG offset and set the offset voltage to -1.3 V. Also, set the output amplitude to 0.8 Vp-p. The offset voltage changes with the change in frequency: plot the error free operation vs. offset voltage range.
The clock bias margin can be measured like this.



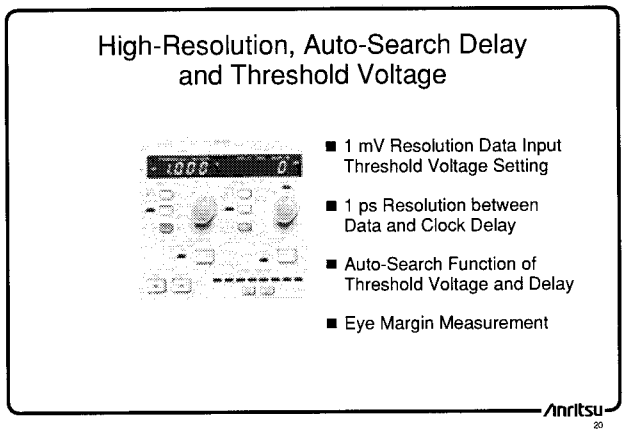
Eight-channel data is provided on the rear panel of the PPG. These outputs' bit rate is 1/8 of fundamental clock.
The application for this output is in testing 8 to 1 multiplexes.



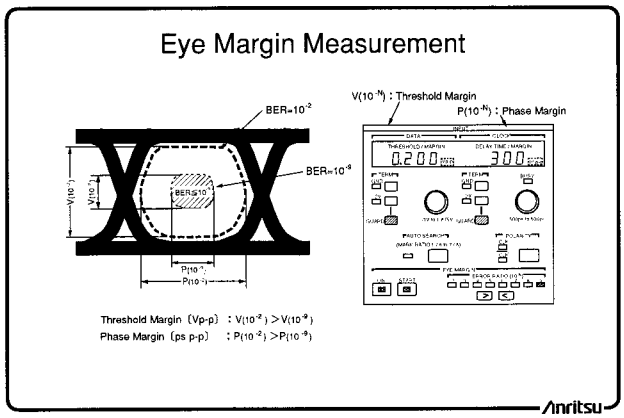
This is the external view of the MP1764C front panel. The layout of the buttons on the front panel are functionally grouped similar to those of the PPG. Only a few functions are assigned to each key or knob in these instruments as is the case with the PPG.



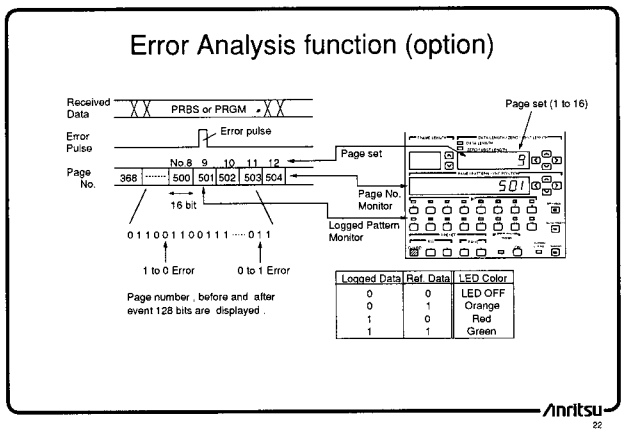
This photograph shows the error detector input section.
The delay and threshold level can be set with high resolution. The delay can be set in 1 ps steps.
The threshold level of Anritsu error detectors can be varied in 1 mv steps. The resolution is sufficient for detecting the minimum error generation point.
The threshold level and delay can be set automatically to the best point using the Auto-Search function. Also, eye margin measurement is possible.



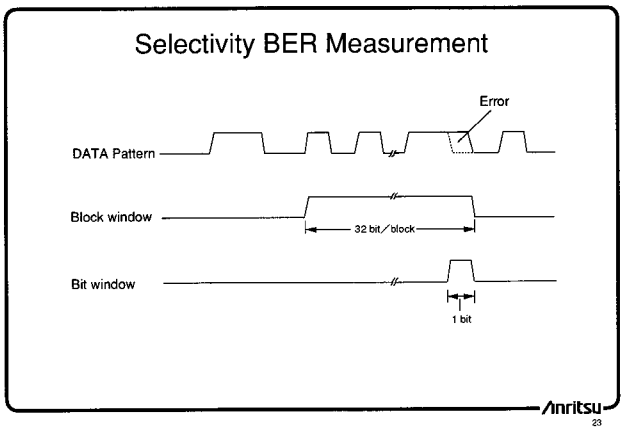
The phase margin and threshold margin can be measured and displayed for an error rate from 10^{-2} to 10^{-9}.



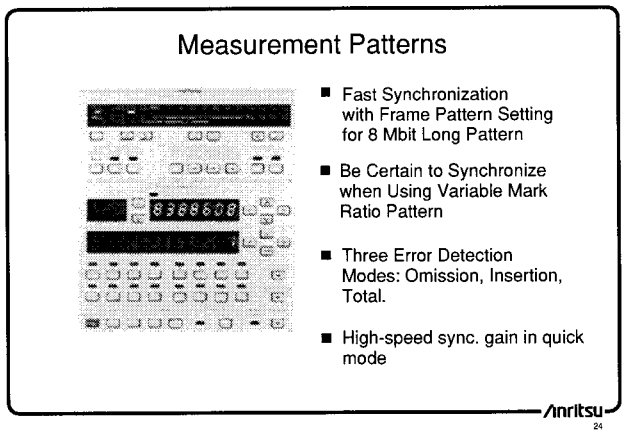
The pattern (256 bits in total) before and after a bit in which an error occurred can be displayed.
Also, insertion and omission errors are displayed using different LED colors.



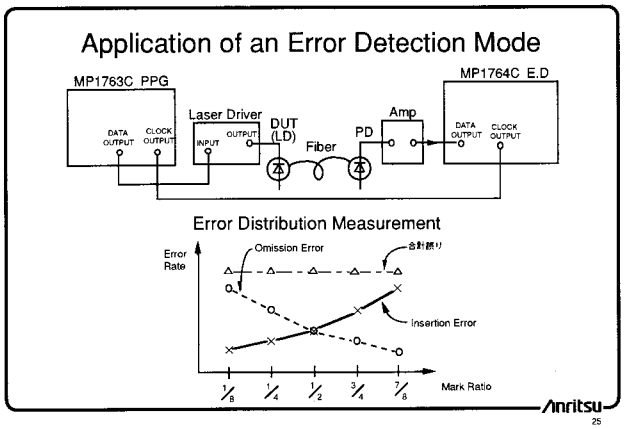
The brock window and bit window are provided.
The bit errors can be measured for any block of 32-bit segments or any bit.



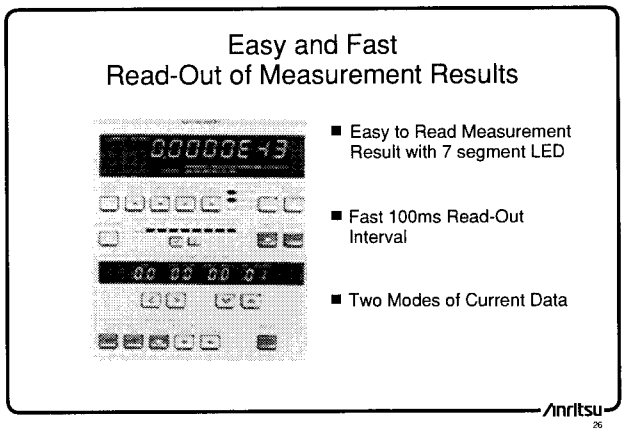
This is the measurement pattern setting section.
All the patterns generated by the PPG can be measured.
However, in error detectors, the biggest problem is the synchronizing time.
Namely, in previous synchronous methods, because the synchronization time is in proportion to the square of the pattern length, if the synchronization time were 1 second for a 512 Kbit pattern, it would be 240 seconds for a 8 Mbit pattern.
The MP1764C has a new synchronization technique which will perform synchronization within a few seconds.
Synchronization is a problem even for the variable mark ratio pattern using PRBS.
Anritsu has found a new synchronous method and has adopted it.
There are three types of error detection mode. If 0 is read as 1, it is called an Insertion error; if 1 is read as 0, it is an Omission error. Both are Total.



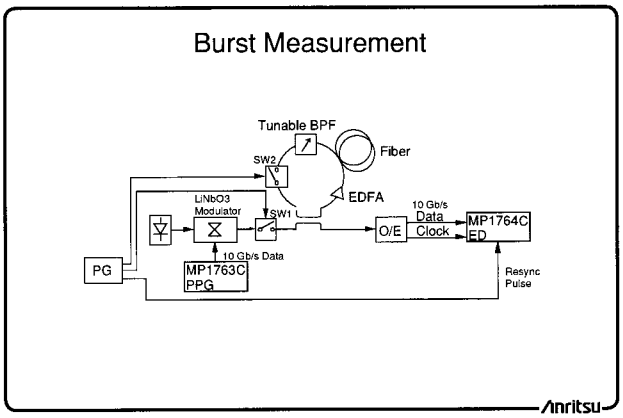
This figure shows the Error Detection Mode application.
In a repeater for optical transmission, sometimes the error rate becomes worse depending on the laser diode emission characteristics. When the diode is off for a long time and is then lit, or when it is on for a long time and then goes off, sometimes the laser diode does not follow-up. The devices with this phenomena should be discriminated.
Normal devices generate Omission and Insertion errors equally, but in devices where these phenomena are striking, the larger value of the Omission or Insertion errors will be obtained.
This application has many uses especially in manufacturing submarine repeater systems.



This is the display section showing the measurement settings and the measured results. The measured results can be read-out easily with the 7-segment LED display.
The measurement gate time can be set to a minimum value of 1 second to a maximum value of 99 days 23 hours 59 min 59 sec in 1 sec step. The Current Data can be read-out with a 100 ms cycle.
Also one of two Current Data Display Cycles can be selected: 100 ms or 200 ms. In addition, there are two Current Data Mode; Interval, and Cycle.



In burst measurements, sync. gain time was much shortened.
The burst error data can be measured even for the PRBS and programmable patterns.
Also, measurement results (error count/error rate) can be displayed on the ED only.



Anritsu

Specifications are subject to change without notice.

ANRITSU CORPORATION
MEASUREMENT SOLUTIONS
5-10-27, Minamiazabu, Minato-ku, Tokyo 106-8570, Japan
Phone: +81-3-3446-1111
Telex: J34372
Fax: +81-3-3442-0235

● **U.S.A.**
ANRITSU COMPANY
North American Region Headquarters
1155 East Collins Blvd., Richardson, Tx 75081, U.S.A.
Toll Free: 1-800-ANRITSU (267-4878)
Phone: +1-972-644-1777
Fax: +1-972-671-1877

● **Canada**
ANRITSU ELECTRONICS LTD.
Unit 102, 215 Stafford Road West
Nepean, Ontario K2H 9C1, Canada
Phone: +1-613-828-4090
Fax: +1-613-828-5400

● **Brasil**
ANRITSU ELETRÔNICA LTDA.
Praia de Botafogo 440, Sala 2401 CEP 22250-040,
Rio de Janeiro, RJ, Brasil
Phone: +55-21-5276922
Fax: +55-21-537-1456

● **U.K.**
ANRITSU LTD.
200 Capability Green, Luton, Bedfordshire LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **Germany**
ANRITSU GmbH
Grafenberger Allee 54-56, 40237 Düsseldorf, Germany
Phone: +49-211-96855-0
Fax: +49-211-96855-55

● **France**
ANRITSU S.A.
9, Avenue du Québec Z.A. de Courtabœuf 91951 Les Ulis Cedex, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Italy**
ANRITSU S.p.A.
Via Elio Vittorini, 129, 00144 Roma EUR, Italy
Phone: +39-06-509-9711
Fax: +39-06-502-24-25

● **Sweden**
ANRITSU AB
Botvid Center, Fittja Backe 1-3 145 84 Stockholm, Sweden
Phone: +46-853470700
Fax: +46-853470730

● **Spain**
ANRITSU ELECTRÓNICA, S.A.
Europa Empresarial Edificio Londres, Planta 1, Oficina 6 C/ Playa de Liencres, 2 28230 Las Rozas. Madrid, Spain
Phone: +34-91-6404460
Fax: +34-91-6404461

● **Singapore**
ANRITSU PTE LTD.
6, New Industrial Rd., #06-01/02, Hoe Huat Industrial Building, Singapore 536199
Phone: +65-282-2400
Fax: +65-282-2533

● **Hong Kong**
ANRITSU COMPANY LTD.
Suite 719, 7/F., Chinachem Golden Plaza, 77 Mody Road, Tsimshatsui East, Kowloon, Hong Kong, China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Korea**
ANRITSU CORPORATION
14F Hyun Juk Bldg. 832-41, Yeoksam-dong, Kangnam-ku, Seoul, Korea
Phone: +82-2-553-6603
Fax: +82-2-553-6604~5

● **Australia**
ANRITSU PTY LTD.
Unit 3/170 Forster Road Mt. Waverley, Victoria, 3149, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**
ANRITSU COMPANY INC.
6F, 96, Sec. 3, Chien Kou North Rd. Taipei, Taiwan
Phone: +886-2-2515-6050
Fax: +886-2-2509-5519

No. MP1763C/1764C-E-E-1-(1.00) 公知 Printed in Japan 2001-4 1AGKD